In the claims:

This listing of the claims will replace all prior versions, and listings, of claims in the application:

Listing of the claims:

1. (Currently amended) A circuit configured to process one or more fibre channel and SCSI frames of data, the circuit comprising:

one or more gates corresponding to a number of bits to be validated that ~~configured to~~ validate format information included in a frame of data with simultaneous bit by bit comparisons, wherein error information is written in the frame of data if an error is found in the format information; and

one or more gates corresponding to a number of bits to be validated that ~~configured to~~ validate command information included in the frame of data with simultaneous bit by bit comparisons, wherein error information is written in the frame of data if an error is found in the command information,

wherein the error information for the format information or command information is used in processing a storage operation for the frame of data,

wherein the validation of the format information and command information is performed at wirespeed.

2. (Original) The circuit of claim 1, wherein the format information comprises fibre channel format information.

3. (Original) The circuit of claim 1, wherein the command information comprises SCSI command information.

4. (Original) The circuit of claim 1, wherein the format information comprises at least one of task attributes, task management, and executive management information.

5. (Original) The circuit of claim 1, wherein the command information comprises opcode information for the storage operation.

6. (Original) The circuit of claim 1, wherein the one or more gates comprise one or more masks that validate the command information.

7. (Withdrawn) A circuit configured to process one or more frames of data, the integrated circuit comprising:

a fibre channel circuit configured to validate a fibre channel header included in a frame of data, wherein error information is written in the frame of data if an error is found in the fibre channel header; and

a SCSI circuit configured to validate a SCSI header included in the frame of data, wherein error information is written in the frame of data if an error is found in the SCSI header,

wherein the error information for the format information or command information is used in processing a storage operation for the frame of data,

wherein the validation of the fibre channel information and SCSI information is performed at wirespeed.

8. (Withdrawn) The circuit of claim 7, wherein the SCSI header comprises an opcode, wherein the SCSI circuit validates whether the opcode is supported.

9. (Currently Amended) A method for processing fibre channel and SCSI frames of data using an integrated circuit, the method comprising:

receiving a frame of data, the frame of data comprising format information and command information;

determining if the format information is valid performing a simultaneous bit by bit comparison of the format information using one or more gates if the format information is not valid, writing error information indicating an error in the format information in the frame of data;

determining if the command information is valid performing a simultaneous bit by bit comparison of the format information using one or more gates and if the command information is

not valid, writing error information indicating an error in the command information in the frame of data,

wherein the error information for the format information or command information is used in processing a storage operation for the frame of data,

wherein determining if the format information valid and determining if the command information is valid is performed at wire speed.

10. (Original) The method of claim 9, wherein determining if the format information is valid comprises checking information in the format information using a circuit that performs the determination at wire speed.

11. (Original) The method of claim 9, wherein determining if the command information is valid comprises checking information in the command information using a circuit that performs the determination at wire speed.